APPLICANT(S): ZHANG, Qi et al.

SERIAL NO.:

10/743,307

FILED:

December 23, 2003

Page 8

REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1-3, 5, 7-16, and 18-25 are pending in the application. Claims 1-3, 5, 7-16, 18and 25 have been rejected. Claims 7-9, 12, 18, and 21 have been amended.

Claims 7 and 8 have been amended to correct a typographical error made in the previous amendment, such that they properly depend from a non-cancelled claim.

Applicants respectfully assert that the amendments to the claims add no new matter.

CLAIM REJECTIONS

35 U.S.C. § 101 Rejections

In the Office Action, the Examiner rejected claims 9-14 and 18-23 under 35 U.S.C. § 101, as being directed to non-statutory subject matter.

Applicants respectfully traverse the rejection, in view of the remarks that follow.

Independent claims 9, 12, 18, and 21 have been amended to clarify that the method or set of stored instructions are both used within the context of a computer or similar electronic computing device (see, e.g., specification, [0039]; Fig. 6), that the resultant integer representation is stored for use as an argument by an instruction in a computer and that a computer instruction using said integer representation as an argument is executed.

Applicants' Specification explains that, according to some embodiments of the claimed invention, the goal of conversion from floating point to integer representation according to the claimed invention is to optimize the conversion of a set of instructions and their associated arguments from a source architecture to a target architecture. See [0003]-

APPLICANT(S): ZHANG, Qi et al.

SERIAL NO.:

10/743,307

FILED:

December 23, 2003

Page 9

[0004], [0020]-[0023]. The converted arguments are executed as part of the target binary code to produce a tangible and useful result in the target architecture. See Fig. 7, 80 and Fig. 8, "target binary code".

Thus, independent claims 9, 12, 18, and 21 produce a resultant output for use in a claimed application, e.g.. executing an instruction in a computing device, and are thus directed to statutory subject matter which does not "consist solely of mathematical operations without some claimed practical application". See MPEP 2106.02 [R-5].

Further, an invention is statutory subject matter under 35 U.S.C. § 101 if it produces a "uscful, tangible, and concrete result." MPEP § 2106.IV.C(2)(2). Clearly executing an instruction in a computing device is useful, as much of the operation of the modern world is based on such processing.

In view of the foregoing amendment and argument, Applicants respectfully request the withdrawal of the 35 USC § 101 rejection from independent claims 9, 12, 18, and 21 in addition to claims 13, 14, 19, 20, 22, and 23, which depend from one of these independent claims.

35 U.S.C. § 103 Rejection

In the Office Action, the Examiner rejected claims 1-3, 5, 7-16, 18-and 25 under 35 U.S.C. § 103(a), as being unpatentable over Yates (2002/0032718) in view of Zohar (2002/087609). Applicants traverse the rejection of claims 1-3, 5, 7-16, 18-and 25 under 35 U.S.C. § 103(a), as being unpatentable over Yates in view of Zohar.

Applicants assert that neither Yates nor Zohar, alone or in combination, teach or suggest, and the Examiner does not assert that Yates or Zohar teach or suggest, "translating the first sequence of instructions into a second sequence of instructions associated with a target architecture, wherein said sequence does not include a floating point control instruction and the translation of said second sequence is conditional on said rounding mode," as claimed in claim 1.

Yates teaches "a computer system for executing a binary image conversion system which converts instructions from an instruction set of a first, non native computer system to a second, different native computing system." (See Yates, abstract.) Zohar teaches a method for APPLICANT(S): ZHANG, Qi et al.

SERIAL NO.:

10/743,307

FILED:

December 23, 2003

Page 10

rounding real numbers. Neither system teaches the above cited claim limitation, such that "said second sequence does not include a floating point control instruction," as claimed in Applicants' claims 1, 15 and 24. At best, the Yates plus Zohar combination teaches a method in which the first sequence of instructions is completely converted into a second sequence of instructions, converting any floating point values into the form required by the target architecture without actually removing the floating point control instruction or performing any rounding by the source architecture. Even if the Yates plus Zohar combination performed floating point to integer rounding according to claims 1, 5, 9, 12, 15, 18, 21, and 24 it would only do so after the first instruction sequence was converted into the second sequence, thereby completely negating any efficiencies gained by Applicants' invention.

Nowhere in the Yates reference does it show that instructions in the source architecture are to be executed by the source architecture, with the resultant value to be converted into the target architecture according to a set rounding mode. The Zohar reference does not cure this deficiency.

Furthermore, the rounding method taught by Zohar does not employ first and second floating point numbers as claimed by independent claims 9, 12, 18, and 21. The method taught by Zohar in Figs. 6-9 employs an entirely distinct series of steps from invention of these claims, as shown by, for example, the embodiment depicted in Figs. 3-5 of the instant Application. Even if the resultant values are equivalent, the implementation and attendant computational costs are entirely distinct.

Each of claims 2, 3, 7, 8, 10, 11, 13, 14, 16, 19, 20, 22, 23, and 25 depends from one of the above mentioned independent claims, includes the limitations of one of those claims, and is therefore allowable for the same reasons

Applicants request that the rejection of claims 1-3, 5, 7-16, 18-and 25 under 35 U.S.C. § 103(a), as being unpatentable over Yates in view of Zohar be withdrawn.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

APPLICANT(S): ZI

SERIAL NO.:

ZHANG, Qi et al. 10/743,307

FILED:

December 23, 2003

Page 11

No fees are believed to be due in conjunction with this paper. However, if any such fees are due, please charge such fees to deposit account No. 50-3355.

Respectfully submitted,

Caleb Pollack

Attorney for Applicants Registration No. 37,912

Dated: October 11, 2007

Pcari Cohen Zedek Latzer, LLP 1500 Broadway, 12th Floor New York, New York 10036 Tel: (646) 878-0800

Fax: (646) 878-0800